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REMARKS

By this Amendment, Applicants have amended the independent claims 11, 13, 15 and 17 to more clearly define their invention. In particular, claims 11, 13, 15 and 17 have been amended to clarify that the trench(es) is/are filled completely with insulating film. This amendment is supported by, e.g., Figure 26 and paragraph 0156 of Applicants' specification. Applicants have also added claims 18-24, corresponding to claims 11-17, respectively, but reciting that the dummy regions are formed at a scribing area with a number, size and layout so that a surface of the element isolation insulating film filled in the trench at the scribing area has a planarized surface, the planarized surface being provided by the polishing and by the number, size and layout of dummy regions. See, e.g., paragraph 0152 and paragraphs 0098-0106 of Applicants' specification.

Claims 11, 13, 15 and 17, as well as claim 14 (and 16?) stand rejected under 35 U.S.C. 103(a) as being unpatentable over by U.S. Patent No. 5,614,445 to Hirabayashi in view of U.S. Patent No. 5,498,565 to Gocho et al and U.S. Patent No. 4,935,800 to Taguchi. Applicants traverse this rejection and request reconsideration thereof.

The rejected claims are directed to a semiconductor integrated circuit device that has at least one trench formed in a semiconductor substrate and a defining active regions and dummy regions. An insulating film completely fills the at least one trench (such that the at least one trench is filled completely with insulating film) by polishing an insulating layer formed over the at least one trench and semiconductor substrate. According to the present invention, the dummy regions are formed at a

scribing area with a number, size and layout so as to planarize a surface of the insulating film formed in the at least one trench at the scribing area by the polishing.

The patent to Hirabayashi discloses a process for manufacturing a semiconductor device that includes forming trench grooves in an integrated circuit region of a wafer and dummy etched grooves in a scribe line zone of a wafer. Both the trench grooves and the dummy etched grooves are provided with a sidewall insulating film on an inner sidewall and are filled with polycrystalline silicon to provide a smooth wafer surface. The wafer is then cleaved along the scribe line zone. The dummy etched grooves are provided so that the sum of the areas to be etched by dry etching accounts for not less than 5% of the total surface area on one side of the wafer.

In Hirabayashi, the insulating film 8 is formed only on the inner sidewalls of the trench and dummy grooves. The trench and dummy grooves of Hirabayashi are not filled completely with the insulating film 8. Rather, the trench grooves and dummy grooves of Hirabayashi are filled with polycrystalline silicon. Thus, the Hirabayashi patent does not disclose an insulating film completely filling a trench or insulating films completely filling a plurality of trenches (such that the at least one trench is filled completely with insulating film) by polishing an insulating layer formed over the trench(es) and the semiconductor substrate, as presently claimed.

Moreover, the purpose of the dummy etched grooves of Hirabayashi is to make the sum of the areas to be etched not less than 5% of the whole area on one side of the semiconductor wafer so as to suppress side etching. On the other hand, the dummy regions of the present invention are formed at a scribing area in a number, size and layout so as to planarize a surface of the insulating films filled in the trenches at the scribing area by the polishing. Thus, the Hirabayashi patent is

not directed to a technique of filling an insulating layer or film in a groove by polishing, e.g., chemical mechanical polishing (CMP) to form an insulating film or layer filled in the groove without dishing, as described at 0152 of Applicants' specification. Thus, this document does not disclose trenches filled completely with an insulating film or layer or dummy regions formed at a scribing area in a number, size and layout so as to planarize a surface of the insulating film(s) filled in the trench(es) at the scribing area by polishing.

Moreover, since the insulating films 8, 8a of Hirabayashi are not completely filling the trenches 6 and since the sidewall insulating film 8, 8a is thin, the breakdown of thin sidewall insulating film can easily occur such that isolation using the polycrystalline silicon 9 may not be sufficient. Thus, characteristics such as parasitic channel (or MOS), the isolation can be reduced and a capacitance between the substrate and the wiring (or aluminum electrode) formed over the substrate is increased, so that the characteristics of the semiconductor integrated circuit device are adversely affected.

Since the purpose and structure of the dummy etched grooves of Hirabayashi are completely different of that of the present invention, it is submitted there would have been no motivation to modify the teachings of Hirabayashi to arrive at the presently claimed invention, i.e., to form the dummy regions, completely filled with insulating film, at the scribing area in a number, size and layout so as to planarize the surface of the insulating film(s) filled in the trench(es) at the scribing area by polishing.

The Gocho et al. patent discloses a method of forming trench isolation including a burying step of burying trenches by a deposition means for conducting etching and deposition simultaneously, and a polishing step of flattening a burying

material by polishing conducted by disposing an isotropic etching step, a multi-layered etching stopper and a protrusion unifying structure. Polishing can be attained with satisfactory flatness uniformly or with no polishing residue even in a portion to be polished in which the etching stopper layer is distributed unevenly. The method can be applied to manufacture of a semiconductor device or the like.

The Gocho et al. patent is directed to a the problems associated with the use of polishing stoppers and polishing steps using polishing stoppers, in particular with respect to the distribution of the polishing stopper layer showing unevenness. Because the portions in which the polishing stoppers are formed are active regions for the device element, the Gocho et al. patent is directed to solving the problem of unevenness of the polishing stopper at a portion of a circuit pattern. See, column 3, lines 16-25 of Gocho et al.

On the other hand, because the scribing area is scribed to form individual chips by cutting a wafer, a large part of the scribing area is removed, so that circuit patterns are not formed in the scribing area. Accordingly, the Gocho et al. patent does not disclose and would not have suggested the use of dummy regions formed at a scribing area.

Moreover, the Hirabayashi et al. patent is a directed to a dry etching technique, and disclosing neither a polishing stopper nor a polishing step. Also, the Hirabayashi patent does not disclose dummy regions formed in a scribing area in a number, size and layout so as to planarize the surface of the insulating film(s) filled in the trench(es) at the scribing area by polishing.

Applicants submit there would have been no motivation to combine the teachings of Hirabayashi and Gocho et al. In Hirabayashi, an insulating material is not completely filled in the trenches. Therefore, it is not clear that the discussion at

column 1, lines 30-55 of Gocho et al., noted by the Examiner in the previous final rejection, is at all relevant to the disclosure of Hirabayashi. Accordingly, it is submitted there would have been no motivation to modify the Hirabayashi teachings to use the deposition and polishing steps of Gocho et al. Moreover, even assuming, arguendo, the teachings of Hirabayashi and Gocho et al. to be combined, the combined teachings would not have suggested the presently claimed invention, including dummy regions, completely filled with insulating film, at a scribing area in a number, size and layout so as to planarizes the surface of the insulating film(s) filled in the trench(es) at the scribing area by the polishing.

The Taguchi patent discloses a semiconductor integrated circuit in which an analog circuit and a digital circuit are formed on a single chip. The semiconductor integrated circuit includes a p-type semiconductor region, an n.sup.+ -type buried region formed on the p-type semiconductor region, an n-type semiconductor region formed on the n.sup.+ -type buried region, a first isolation portion, extending through the n-type semiconductor region and the n.sup.+ -type buried region and reaching the p-type semiconductor region, for isolating adjacent transistors in an analog circuit formed on the n-type semiconductor region, and a second isolation portion, formed in the n-type semiconductor region, for isolating adjacent transistors in the n-type semiconductor region.

While the Examiner cites Taguchi as allegedly teaching a trench isolation in which oxide completely fills the trench, the Taguchi patent does not disclose this feature. Rather trenches 17 and 19 have an undoped silicon oxide film 20 deposited on only the wall surfaces of the trenches and an undoped polysilicon layer 25 deposited to completely fill the trenches and then etched. Thus, the oxide layers in Taguchi are not completely filling the trenches. Accordingly, nothing in Taguchi

remedies any of the deficiencies noted above with respect to Hirabayashi and Gocho et al.

In view of the foregoing amendments and remarks, favorable reconsideration and allowance of all the claims now in the application are request.

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To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 1374.36127CC3), and please credit any excess fees to such deposit account.

Respectfully submitted,

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